Amendments to the Claims:

A clean version of the entire set of pending claims, including amendments to the claims, is submitted herewith per 37 CFR 1.121(c)(3). This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A coprocessor coupled to a main processor having an execution speed greater than that of said processor, the coprocessor comprising a two-dimensional array of processing cells, including a plurality of periphery cells located on peripheral sides of the array; and

~~and being communicatively connected to said processor by~~ an interface module, comprising: ~~having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array;~~

a plurality of input/output pads for the coprocessor,

a plurality of border cells disposed along an outside of the two-dimensional array, each border cell being connected to a corresponding one of the periphery cells, each border cell including a buffer, and

a crossbar network for reconfigurably connecting each of the I/O pads to one of the border cells.

2. (Previously Presented) The coprocessor of claim 1, wherein the array comprises a systolic processing array.

3. (Canceled)

4. (Previously Presented) The coprocessor of claim 1, wherein the coprocessor performs mathematical operations whose timing is based on a flow of input operands along the paths.

5. (Previously Presented) The coprocessor of claim 1, wherein inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent.

6. (Previously Presented) A coprocessing system including the coprocessor, interface module and main processor of claim 1 and a shared memory that communicatively connects with the interface module and the main processor to provide the main processor to coprocessor connection.

7. (Previously Presented) The coprocessor of claim 1, including an array processor that comprises said two-dimensional array.

8. (Previously Presented) An integrated circuit comprising the coprocessor of claim 1.

9-12. (Canceled)

13. (Currently Amended) A functional unit having a two-dimensional array of processing cells and ~~serving as a component of~~being coupled to a main processor, the unit having a mechanism external to the two-dimensional array for reconfiguring a plurality of intra-processor information paths to the array to respective cells on a periphery of the array.

14. (Canceled)

15. (Previously Presented) The unit of claim 13, wherein inter-cell connection within the array is such that each cell of the array is connected only to cells whose column is the same and whose row is immediately adjacent, and only to cells whose row is the same and whose column is immediately adjacent.

16. (Previously Presented) The unit of claim 13, further including means for transmitting a plurality of array programs to corresponding predetermined subsets of said processing cells.

17. (Currently Amended) A system including the ~~processor~~ functional unit of claim 16, and an array program generator for generating array programs to be transmitted, and, when needed, updating a program, transmitting the updated program, and transmitting concurrently, when needed, a reconfigure signal to said mechanism to correspondingly update a current steady state connection pattern of said information paths.

18. (Previously Presented) The system of claim 17, further including a compiler configured for receiving, in response to said program updating, data representative of input and output timing for said unit and further configured for compiling an instruction based on said data.

19. (Canceled)

20. (Previously Presented) A method for interfacing a coprocessor to a main processor, comprising the steps of:

configuring the coprocessor to compromise a two-dimensional array of processing cells and to have an execution speed greater than that of said processor; and

communicatively connecting the coprocessor to said processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array.

21. (Previously Presented) The coprocessor of claim 1, wherein the array is rectangular, wherein the periphery consists of those of said processing cells located

in all of a first row, last row, first column and last column of said array, and wherein the interface module's mechanism for reconfiguring a plurality of information paths reconfigures information paths directly connecting the interface module and each of the cells on the periphery of the array.

22. (Previously Presented) The coprocessor of claim 1, wherein the interface comprises a plurality of border cells directly connected to the respective processing cells on the periphery of the array.

23. (Previously Presented) The coprocessor of claim 1, further comprising a master cell for forwarding array programs to the processing cells of the two-dimensional array.

24. (New) The functional unit of claim 13, wherein the mechanism for reconfiguring the plurality of intra-processor information paths to the array to respective cells on the periphery of the array comprises:

a plurality of input/output pads for the functional unit,

a plurality of border cells disposed along an outside of the two-dimensional array, each border cell being connected to a corresponding one of the periphery cells, each border cell including a buffer, and

a crossbar network for reconfigurably connecting each of the I/O pads to one of the border cells.

25. (New) The method of claim 20, wherein communicatively connecting the coprocessor to said processor by an interface module having a mechanism for reconfiguring a plurality of information paths between the interface module and respective cells on a periphery of the array comprises:

providing a plurality of input/output pads for the coprocessor,

providing plurality of border cells disposed along an outside of the two-dimensional array, each border cell being connected to a corresponding one of the

periphery cells, each border cell including a buffer, and

employing a crossbar network to reconfigurably connect each of the I/O pads to one of the border cells.